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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,555	07/26/2001	Chih-Hsin Wang	2102397-911400	8544

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EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	

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12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/916,555	Applicant(s) WANG ET AL.
	Examiner Marcos D. Pizarro-Crespo	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Attorney's Docket Number: 2101397-911400

Filing Date: 7/26/2001

Claimed Priority Dates: 4/26/2001 (Provisional 60/287,047)
3/12/2001 (Provisional 60/275,517)
1/5/2001 (Provisional 60/242,096)
9/20/2000 (Provisional 60/234,314)

Applicant(s): Wang et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 12 filed on 2/20/2003.

Continued Examination Under 37 CFR 1.114

1. A request for a continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the final rejection in paper no. 10, mailed on 11/29/2002. Since this application is eligible for a continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/20/2003 has been entered.

Acknowledgment

2. The amendment in paper no. 12 filed on 2/20/2003 in response to Office action mailed in paper no. 10, mailed on 11/29/2002, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 27-45.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 27-30, 37, and 39-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Taketa (US 5939749).

5. Regarding claim 27, Taketa (see, *e.g.*, fig. 6) shows all aspects of the instant invention including an electrically programmable and erasable memory device comprising:

- a substrate **2** of semiconductor material of a first conductivity type (p-type)
- first **3** and second **4** spaced-apart regions of a second conductivity type (n-type)
- a channel region **5** between the first **3** and second **4** spaced-apart regions
- an electrically conductive floating gate **32** disposed over and insulated from a portion of the channel region **5** and a portion of the first region **3**, wherein the floating gate consists of a first portion and a second portion integrally formed together
- an electrically conductive source region **14** disposed over and electrically connected to the first region **3**, the source region having:
  - a lower portion disposed adjacent to and insulated from the floating gate

- an upper portion of the source region **14** disposed over and insulated from the first portion of the floating gate **32** and not the second portion of the floating gate **32**

➢ an electrically conductive control gate **9** having a first portion and a second portion

wherein:

➢ the first portion of the control gate **9** is adjacent to and insulated from the floating gate **32**, and

➢ the second portion of the control gate **9** is over and insulated from the second portion of the floating gate **32** and not the first portion of the floating gate **32**

6. Regarding claim 28, Taketa (see, *e.g.*, fig. 6) shows that the upper portion of the source-region **14** is wider than the lower portion of the source-region **14**.

7. Regarding claim 29, Taketa (see, *e.g.*, fig. 6) shows the source region **14** having a substantially T-shaped cross-section.

8. Regarding claims 30 and 41, Taketa (see, *e.g.*, fig. 6) shows the memory device further comprising an insulation layer **8** disposed between the floating gate **32** and the control gate **9** and a having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (col.9/ll.37).

9. Regarding claim 37, Taketa (see, *e.g.*, fig. 6) shows the memory device further comprising insulation material **15** between the upper portion of the source region **14** and the first portion of the floating gate **32**, and having a thickness permitting voltage coupling therebetween.

10. Regarding claim 39, Taketa shows all aspects of the instant invention including an electrically programmable and erasable memory device comprising:

- a substrate **2** of semiconductor material of a first conductivity type (p-type)
- first **3** and second **4** spaced-apart regions of a second conductivity type (n-type)
- a channel region **5** between the first **3** and second **4** spaced-apart regions
- an electrically conductive floating gate **32** disposed over and insulated from a portion of the channel region **5** and a portion of the first region **3**
- an electrically conductive source region **14** electrically connected to the first region **3**, the source region having:
  - a lower portion disposed adjacent to and insulated from the floating gate **32**
  - an upper portion disposed over and insulated from the floating gate **32**
- an electrically conductive control gate **9** having a first portion and a second portion

wherein:

- the first portion of the control gate **9** is adjacent to and insulated from the floating gate **32**, and
- the second portion of the control gate **9** is over and insulated from the floating gate **32** and not the first portion of the floating gate **32**
- the source region upper portion is adjacent to and insulated from the control gate second portion, with no vertical overlap between the portions

11. Regarding claim 40, Taketa (see, *e.g.*, fig. 6) shows the memory device further comprising insulation material **15** between the upper and lower portions of the source region **14** and the floating gate **32**, and having a thickness permitting voltage coupling therethrough.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 31-36, 38, and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taketa in view of Kao (US 6211547).

15. Taketa (see, *e.g.*, fig. 6) shows most aspects of the instant invention including an array of electrically programmable and erasable memory devices comprising:

- a substrate **2** of semiconductor material of a first conductivity type (p-type)
- a plurality of active regions (see, *e.g.*, the cross-sectional view in fig. 6 and the circuit diagram in fig. 11), each of the active regions including a column of pairs **31a 31b** of memory cells extending in a first direction, each of the memory cell pairs **31a 31b** including:
  - a first region **3** and a pair of second regions **4** spaced apart in the substrate **2** and of a second conductivity type (n-type)
  - channel regions **5** between the first region **3** and the second regions **4**
  - a pair of electrically conductive floating gates **32**, each disposed over and insulated from a portion of the channel regions **5** and a portion of the first region **3**, wherein each of the floating gates consists of a first portion and a second portion integrally formed together
  - an electrically conductive source region **14** disposed over and electrically connected to the first region **3** in the substrate **2**
  - a lower portion of the source region **14** that is disposed adjacent to and insulated from the pair of floating gates **32**
  - an upper portion of the source region **14** that is disposed over and insulated from the first portions of each of the floating gates **32** and not their second portions
  - a pair of electrically conductive control gates **9** each having a first portion and a second portion

wherein for each of the control gates **9**:

- the first portion is adjacent to and insulated from one of the floating gates **32**, and
- the second portion is over and insulated from the second portion and not the first portion of said one of the floating gates **32**

However, the cross-sectional views of the memory-cell arrays in Taketa's drawings (see, *e.g.*, fig. 6) fail to show spaced-apart isolation regions parallel to one another in the first direction such that each active region is between a pair of adjacent isolation regions. Nonetheless, the skilled artisan will understand that a cross-sectional view perpendicular to Taketa's drawing in figure 6 will show such isolation regions. See, *e.g.*, figs. 1-3 of Kao, where he shows conventional memory-cell arrays similar to Taketa's. A top view (see, *e.g.*, fig. 3) of Kao's conventional structure shows spaced-apart isolation regions (FOX) parallel to one another in a first direction such that an active region, similar to the one in figure 6 of Taketa, is between each pair of adjacent isolation regions. Moreover, Kao teaches (col.3/ll.11-15) that such isolation regions are conventionally used in the art to separate adjacent columns of memory-cell transistors.

Accordingly, it would have been obvious to one of ordinary skill in the art that Taketa's memory device includes spaced apart isolation regions parallel to one another in the first direction such that an active region is between each pair of adjacent isolation regions, as taught by Kao, since such isolation regions are conventionally used in the art to separate adjacent columns of memory-cell transistors, *i.e.*, active regions.

16. Regarding claim 32, Taketa (see, *e.g.*, fig. 6) shows that upper portion of the source-region **14** is wider than the lower portion of the source-region **14**.

17. Regarding claim 33, Taketa (see, *e.g.*, fig. 6) shows the source region **14** having a substantially T-shaped cross-section.

18. Regarding claim 34 and 43, Taketa (see, *e.g.*, fig. 11) shows the source region **14** of each of the memory-cell pairs **31a 31b** extending in a second direction substantially perpendicular to the first direction such that it intercepts a pair **31a 31b** of memory cells in each of the active regions. Kao (see, *e.g.*, fig. 3) shows the isolation regions (FOX) parallel to the first direction.

19. Regarding claims 35 and 45, Taketa (see, *e.g.*, fig. 6) shows the memory device further comprising an insulation layer **8** disposed between each of the floating gates **32** and each of the control gates **9** having a thickness permitting Fowler-Nordheim tunneling of charges therethrough (col.9/ll.37).

20. Regarding claim 36, Taketa (see, *e.g.*, fig. 11) shows each of the control gates **9** extending across the active regions in a second direction substantially perpendicular to the first direction and intercepting one of the memory-cell pairs **31a 31b** in each of the active regions. Kao (see, *e.g.*, fig. 3) shows the isolation regions (FOX) parallel to the first direction.

21. Regarding claim 38, Taketa shows (see, *e.g.*, fig. 6) each of the memory cell pair **31a 31b** further comprising an insulation material **15** between the upper portion of the source region **14** and each of the first portions of the floating gates **32**, and having a thickness permitting voltage coupling therebetween.

22. Regarding claim 42, Taketa (see, *e.g.*, fig. 6) shows most aspects of the instant invention including an array of electrically programmable and erasable memory devices comprising:

- a substrate **2** of semiconductor material of a first conductivity type (p-type)
- a plurality of active regions (see, *e.g.*, the cross-sectional view in fig. 6 and the circuit diagram in fig. 11), each of the active regions including a column of pairs **31a 31b** of memory cells extending in a first direction, each of the memory cell pairs **31a 31b** including:
  - a first region **3** and a pair of second regions **4** spaced apart in the substrate **2** and of a second conductivity type (n-type)
  - channel regions **5** between the first region **3** and the second regions **4**
  - a pair of electrically conductive floating gates **32**, each disposed over and insulated from a portion of the channel regions **5** and a portion of the first region **3**
  - an electrically conductive source region **14** electrically connected to the first region **3**, the source region having:
    - a lower portion that is disposed adjacent to and insulated from the pair of floating gates **32**
    - an upper portion that is disposed over and insulated from the floating gates **32**
  - a pair of electrically conductive control gates **9** each having a first portion and a second portion

wherein for each of the control gates **9**:

- the first portion is adjacent to and insulated from one of the floating gates **32**, and
- the second portion is over and insulated from the one of the floating gates **32**
- each of the second portions is adjacent to and insulated from the source region upper portion with no vertical overlap between the portions

However, the cross-sectional views of the memory-cell arrays in Taketa's drawings (see, *e.g.*, fig. 6) fail to show spaced-apart isolation regions parallel to one another in the first direction such that each active region is between a pair of adjacent isolation regions. Nonetheless, the skilled artisan will understand that a cross-sectional view perpendicular to Taketa's drawing in figure 6 will show such isolation regions. See, *e.g.*, figs. 1-3 of Kao, where he shows conventional memory-cell arrays similar to Taketa's. A top view (see, *e.g.*, fig. 3) of Kao's conventional structure shows spaced-apart isolation regions (FOX) parallel to one another in a first direction such that an active region, similar to the one in figure 6 of Taketa, is between each pair of adjacent isolation regions. Moreover, Kao teaches (col.3/ll.11-15) that such isolation regions are conventionally used in the art to separate adjacent columns of memory-cell transistors.

Accordingly, it would have been obvious to one of ordinary skill in the art that Taketa's memory device includes spaced apart isolation regions parallel to one another in the first direction such that an active region is between each pair of adjacent isolation regions, as taught by Kao, since such isolation regions are conventionally used in the art to separate adjacent columns of memory-cell transistors, *i.e.*, active regions.

23. Regarding claim 44, Taketa shows (see, *e.g.*, fig. 6) each of the memory cell pair **31a 31b** further comprising an insulation material **15** between the upper and lower portions of the source region **14** and the pair of floating gates **32**, and having a thickness permitting voltage coupling therethrough.

Response to Arguments

24. The applicants argue:

> Claim 27 recites that the floating gate consists of first and second portions integrally formed together, where the conductive source region is disposed over and insulated from the floating gate first portion *and not the floating gate second portion*, and the control gate second portion is disposed over and insulated from the floating gate second portion *and not the floating gate first portion*. No matter how one divides the claimed floating gate into the integrally formed first and second portions recited in claim 27, no portion of the floating gate can have both the source region upper portion and the control gate second portion disposed over it. Taketa fails to show these limitations in the claim.

The examiner argues:

Taketa clearly shows all the limitations recited in claim 27. See, for example, figure 6, where Taketa clearly shows the floating gate **32** consisting of a first and a second portion integrally formed together. Taketa further shows in figure 6 that the upper portion of the source region **14** is over and insulated from the first portion of the floating gate **32** *and not the second portion of the floating gate* **32**, and that a second portion of the control gate is over and insulated from the second portion of the floating gate *and not the first portion of the floating gate* **32**. Also in figure 6, Taketa further shows that no portion of the floating gate has both the source region upper portion and the control gate second portion disposed over it.

25. The applicants argue:

> Amended claim 37 recites that the insulation material between the source region upper portion and the floating gate first portion has a thickness for permitting voltage coupling between these portions. Taketa's structure clearly precludes voltage coupling between the source region upper portion and the floating gate.

The examiner responds:

Voltage coupling between portions of a circuit occurs when the portions are somehow joined so as to enable a voltage signal to be transferred from one portion to the other. Taketa clearly shows that voltage coupling occurs between the source region upper portion and the floating gate first portion. See, *e.g.*, col.9/ll.52-55.

Conclusion

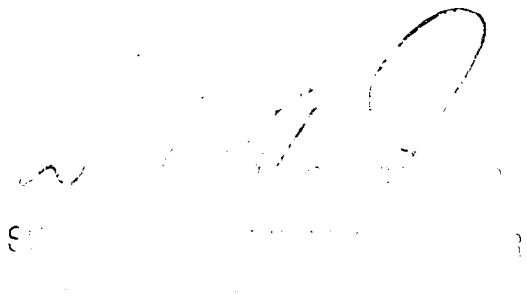
26. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

28. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

29. The following list is the Examiner's field of search for the present Office action:

Field of Search	Date
U S Class / Subclass(es) 257/314-326	3/13/2003
Other Documentation PLUS Analysis	7/17/2002
Electronic Database(s) EAST (USPAT, EPO, JPO)	3/13/2003



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